

GENERAL DESCRIPTION

The CORE-H110-TDM provides a fully H.110 Compatible TDM Switch solution suited to H.110 TDM bus based systems. This Core is targeted to applications processing E1/T1/J1 data, providing a Backplane Interface and two PTMC Site Interfaces. Switching is performed at the E1 level, in sets of 32 Timeslots. A dual-bank Connection Memory enables hitless switching when altering stream mappings. Additionally, an on-board framer synchronises the incoming frame pulse to prevent loss of Switch synchronisation due to frame pulse jitter. The Core operates in constant-latency mode, enabling use in N x 64 applications where data is transmitted over multiple timeslots.

FUNCTIONAL DESCRIPTION

H.110 Interface

The H.110 Interface operates with an 8.192MHz Clock and an 8KHz Frame Pulse. 32 Streams are provided per Interface, each one carrying 128 channels. This allows for a total of 4,096 channels per Interface. The Core acts as a Slave on the Backplane Interface, taking the Backplane Clock and Frame Pulse as inputs for timing purposes. On the PTMC Interfaces, the Core provides Clock and Frame pulse outputs, which are synchronised to the Backplane Clock and Frame Pulse.

The Core requires an external 8X PLL to increase the Backplane Clock from 8.192MHz to 65.536MHz prior to the FPGA device. If targeted to devices other than the Spartan-2E, the on-board DCM may be used instead providing clock jitter requirements are met.

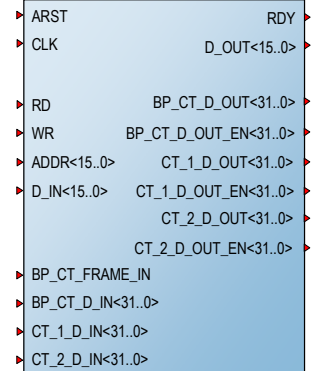
Each Stream is fully bidirectional. For each Stream I/O pin, the Core provides an Input, Output and Output Enable signal. Technology-specific I/O Cells are instantiated in the top-level wrapper file, supplied with the Core.

Switch Operation

The Core provides the ability to route sets of 32 Timeslots, referred to as a Timeslot Group between any two Interfaces. It is also possible to loopback Timeslot Groups on either PTMC Interface. The Core always delays data by two frames, regardless of the source and destination routing. Dual Connection Memories are provided, with a mechanism to perform a transition between them on a frame boundary. The Core operates at 65.536MHz, derived from an external PLL. The incoming Backplane Frame Pulse passes through a framer which will reject any jitter present with respect to the 65.536MHz clock input. The state of the framer may be read via the CPU Interface, it may also be reset at any time.

INTERFACE CONFIGURATION

TDM Switch



FEATURES

- **H.110 Bus Compliant**
 - 32 Streams supported
 - 8.192MHz Stream Rate
 - 4,096 Channels per Interface
- **Backplane Interface and two PTMC Site Interfaces**
- **Generic Memory Interface**
- **Constant Latency**
- **Dual Connection Memory**
- **Targets Xilinx Spartan FPGA for low cost.**

TARGET APPLICATIONS

- **CompactPCI H.110 Systems**
- **Backplane Interfaces**

BLOCK DIAGRAM

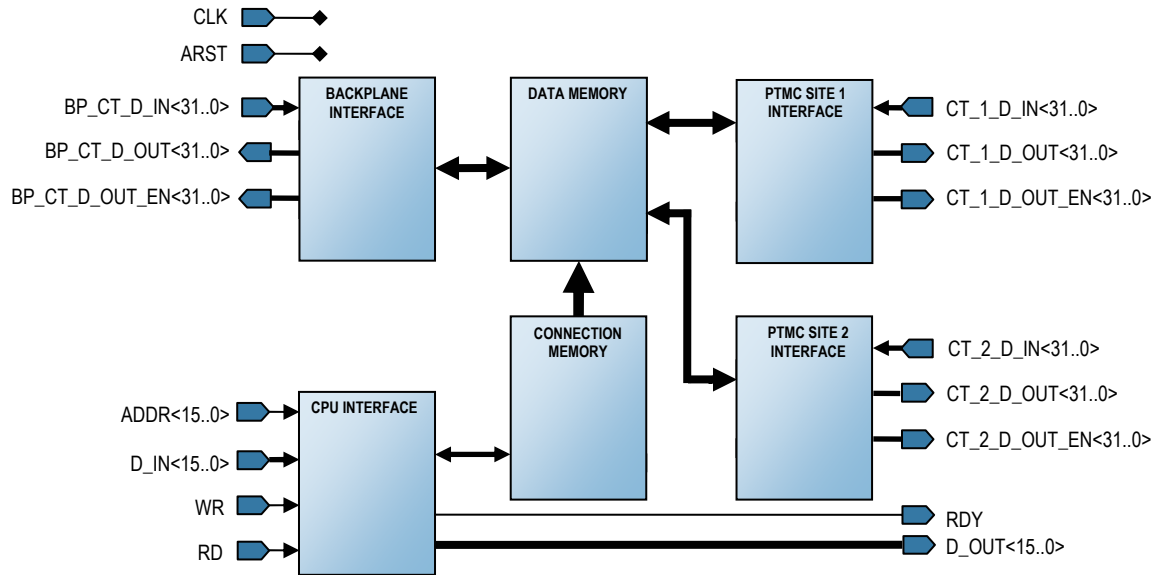


Figure 1 Block Diagram

FUNCTIONAL DESCRIPTION (CONT...)

CPU Interface

The CPU interface provides the control and status access for the core. A generic interface has been designed to allow simple connection to the many processor buses available. The interface is synchronous to the Backplane clock (CLK) and consists of a 16 bit address bus (ADDR), 16 bit input data bus (D_IN), 16 bit output data bus (D_OUT), transaction ready output (RDY), read enable (RD) and write enable (WR).

A read cycle is achieved by asserting RD for one clock cycle while supplying a valid address. When the RDY output pulses the data may be read from D_OUT. A write cycle is achieved by asserting WR for one clock cycle while supplying valid address and data. Once the bus transaction is complete, the RDY output will pulse for one clock cycle.

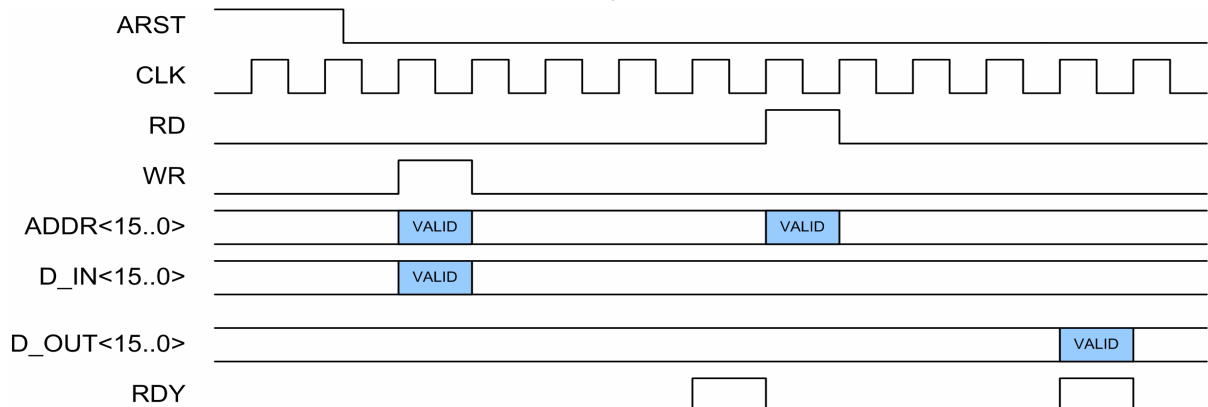
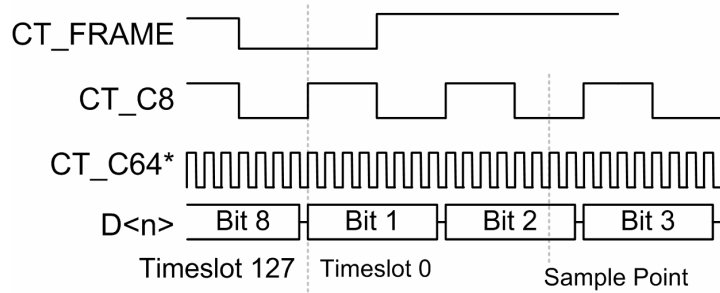


Figure 2 Example CPU Cycles

H.110 Bus Timing

The frame pulse is compared with the expected location of the frame header to determine Out of Frame (OOF) and Loss of Frame (LOF) alarms. OOF and LOF status is accessible via the statistics module. Frame re-alignment can be forced via the CPU interface.

H.110 Bus Data Format



* Supplied by external PLL

Figure 3 H.110 Bus Data Format

The Core processes Timeslots in groups of 32. The grouping for each Stream is as follows:

Timeslots	Group
0-31	0
32-63	1
64-95	2
96-127	3

For the Backplane, an external Bus Master must provide the Clock and Frame Pulse. These act as inputs into the Core, controlling internal timing and the PTMC Site timing. Each PTMC Site must be configured as an H.110 Slave, accepting the provided Clock and Frame Pulse.

INTERFACE DESCRIPTION

Symbol	I/O	Level	Description
ARST	I	H	Asynchronous reset for all modules
CLK	I	CP	System clock supporting frequencies up to 155.52MHz
RD	I	H	Initiates a Read transaction
WR	O	H	Initiates a Write transaction
ADDR<15..0>	I	X	Address to access
D_IN<15..0>	I	X	Data to write to the Core
D_OUT<15..0>	I	X	Data read from the Core
RDY	I	H	Transaction is complete
BP_CT_FRAME_IN	I	H	Backplane Frame In
BP_CT_D_IN<31..0>	I	X	Backplane Stream Inputs
BP_CT_D_OUT<31..0>	O	X	Backplane Stream Outputs
BP_CT_D_OUT_EN<31..0>	O	X	Backplane Stream Output Enables
CT_1_D_IN<31..0>	I	X	PTMC Site 1 Stream Inputs
CT_1_D_OUT<31..0>	O	X	PTMC Site 1 Stream Outputs
CT_1_D_OUT_EN<31..0>	O	X	PTMC Site 1 Stream Output Enables
CT_2_D_IN<31..0>	I	X	PTMC Site 2 Stream Inputs
CT_2_D_OUT<31..0>	O	X	PTMC Site 2 Stream Outputs
CT_2_D_OUT_EN<31..0>	O	X	PTMC Site 2 Stream Output Enables

KEY: I = INPUT, O = OUTPUT, C = CLOCK, P = POSITIVE EDGE SENSITIVE, N = NEGATIVE EDGE SENSITIVE, H = ACTIVE HIGH, L = ACTIVE LOW, X = BUS

H.110 Interfacing Requirements

In a CompactPCI system, the cards are hot-swappable. To support this, a FET Bus Switch such as the IDTQS34X2245 must be used to isolate the FPGA pins from the Backplane Connector. Additionally, the Backplane H.110 lines must be pre-charged to 0.7V via 18K resistors using CompactPCI Early Power to properly support Hot Swap operation. Refer to the *ECTF H.110 Hardware Compatibility Specification: CT Bus* for more information. The PTMC Modules are not hot-swappable and therefore do not require special pre-charging circuitry.

NOTES
Design Detail

This data sheet provides a general overview of the CORE-H110-TDM. For further technical details including CPU memory map, CPU register definitions and detailed timing diagrams, please contact CALYPTTECH via one of the methods detailed below.

Implementation

The CORE-H110-TDM is available as an EDIF net-list file or VHDL source code, with a constraint file to achieve routing at maximum speed. A VHDL test bench can be supplied to verify operation of the provided implementation of the CORE-H110-TDM.

Scripts are provided to illustrate the usage of the Connection memory of this Core.

CALYPTTECH CONTACT DETAILS

Support and technical assistance is available for all CALYPTTECH Intellectual Property cores.

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