

GENERAL DESCRIPTION

The CORE-PM-2G5 provides multi-rate performance monitoring for several standard protocols including SONET, SDH, Fibre Channel and Gigabit Ethernet.

The performance monitoring for SONET/SDH modes includes line and section overhead processing at the following rates;

- STS-3/STM-1 (OC3)
- STS-12/STM-4 (OC12)
- STS-48/STM-16 (OC48)

In addition 8B / 10B processing supports Fibre Channel and Gigabit Ethernet protocols.

The core is configured via a generic CPU interface, allowing the data rate and mode of operation (SONET/SDH or 8B/10B) to be selected. For each mode of operation a set of performance statistics is maintained that is accessible via the CPU interface.

FUNCTIONAL DESCRIPTION

Front End Interface

The core receives data from the incoming data stream synchronous to the core system clock. Core operating frequencies up to 155.52MHz combined with flexible input bus widths of 4, 8, 10 and 16 bits provide support for data rates up to 2.488 Gb/s.

The front end interface incorporates the de-multiplexing module which translates the external data bus into a 16 bit internal data bus with corresponding data valid strobe. The active input data signals are centred within the 16 bit input bus when bus widths other than 16 bit are selected. The 10 bit bus width is only supported when operating in 8B/10B mode. When a 10 bit bus is selected, the data is contained in the 10 LSBs of the internal data bus. The de-multiplexer ratio is configured via the CPU interface.

A frame pulse input is used to indicate frame boundaries for both SONET/SDH and 8B/10B modes of operation.

Bus Width	Active Inputs
4	DATA9..D6
8	DATA11..D4
10	DATA12..D3
16	DATA15..D0

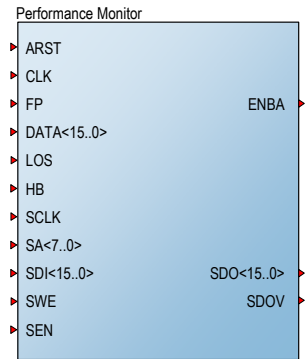
SONET / SDH Alignment

In SONET/SDH mode with a 16 bit bus width, the frame pulse is expected to be aligned with the first two A2 octets within the standard SONET/SDH frame header. Selecting an 8 bit bus requires the frame pulse to be aligned with the first A2 octet whilst a 4 bit bus requires alignment to the most significant nibble of the first A2 octet.

A byte alignment output (ENBA) is provided to enable an external pattern matcher to byte align the data stream to the SONET/SDH frame. ENBA is asserted whilst the core is seeking frame alignment.

Once frame alignment has been detected, via the frame pulse, a row and column count is generated to identify the location of specific overhead octets within the SONET/SDH Frame. Comparators, configured via the CPU interface, are implemented to match on these key octets to enable correct OC3, OC12 and OC48 overhead extraction.

INTERFACE CONFIGURATION



FEATURES

- Data rates up to 2.488Gb/s
- OC-3, OC-12, OC48, GbE, FC
- SONET / SDH Processing
 - Loss of Signal Status
 - Frame Alignment Status
 - B1 Error Count
 - B2 Error Count
 - AIS Status
 - RDI Status
 - REI Status
 - M1 Octet Capture
 - K1 / K2 Octet Capture
 - J0 Octet Capture
- 8B / 10B Processing
 - Loss of Signal Status
 - Loss of Sync Status
 - Invalid Code Status
 - Disparity Error Status
 - Loss of Sync Count
 - Invalid Code Count
 - Disparity Error Count
- CPU Interface
- Suitable for FPGA or ASIC

TARGET APPLICATIONS

- Performance Monitoring
- Network Analyser

BLOCK DIAGRAM

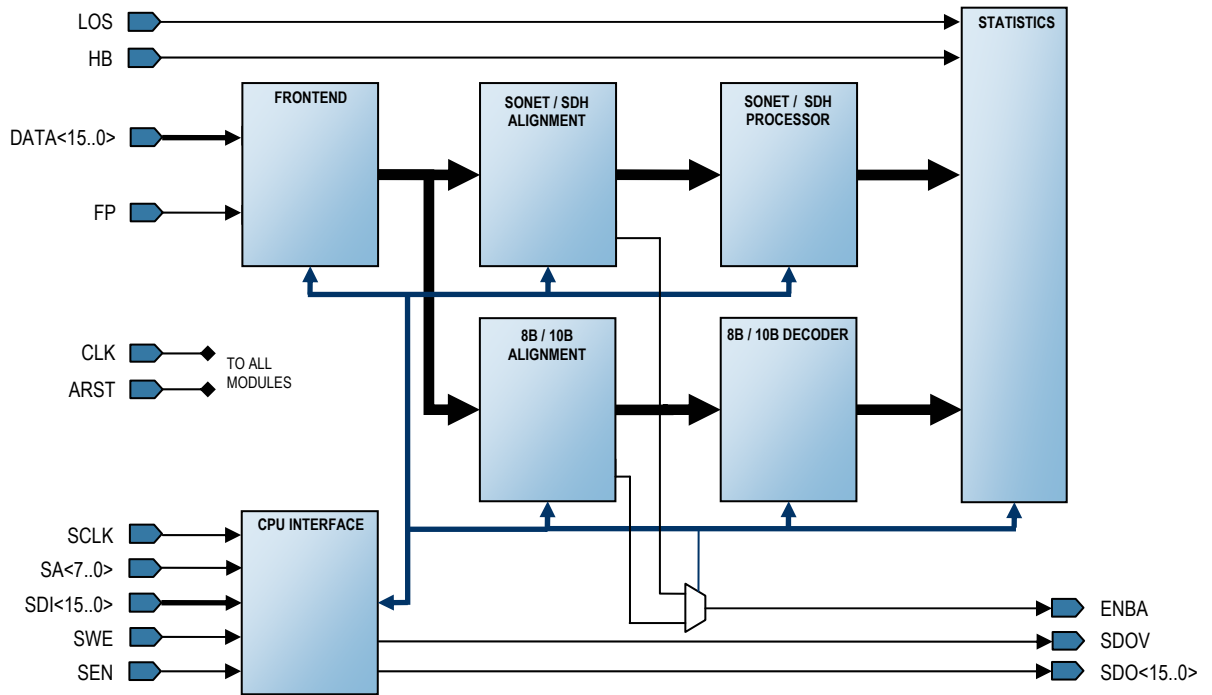


Figure 1 Block Diagram

FUNCTIONAL DESCRIPTION

SONET / SDH Alignment Cont..

The frame pulse is compared with the expected location of the frame header to determine Out of Frame (OOF) and Loss of Frame (LOF) alarms. OOF and LOF status is accessible via the statistics module. Frame re-alignment can be forced via the CPU interface.

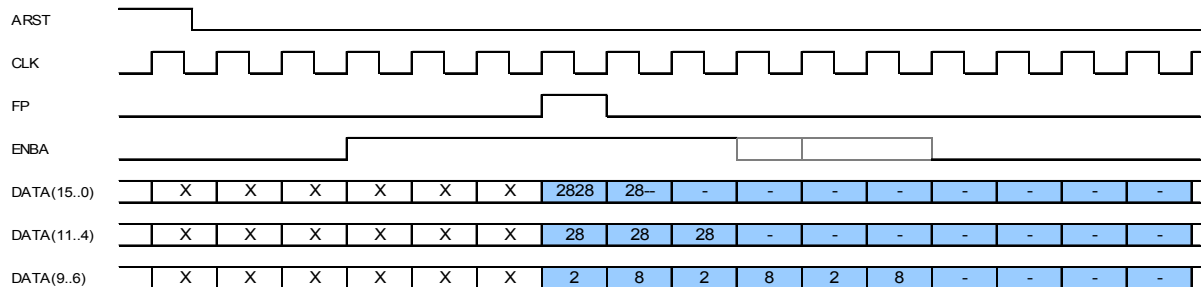


Figure 2 SONET / SDH Frame Alignment

SONET / SDH Performance Monitoring

The B1 octet located in the section/regenerator overhead of the SONET/SDH frame is extracted to determine B1 errors. The B1 calculation is a Bit Interleaved Parity 8 (BIP-8) calculation on each data bit in the frame. The parity calculation is performed over the entire SONET/SDH frame including both payload and overhead octets before descrambling has occurred. At the end of each frame the running calculation is compared with the extracted B1 octet and an error count is generated. The error count can be selected via the CPU interface, to provide either a bit count or a block count. The B1 error count is passed to the statistics module and is only updated when the LOF alarm is negated.

Descrambling of the incoming data stream is performed before further processing of the SONET/SDH frame occurs. The descrambler is implemented using the standard SONET/SDH polynomial of X^7+X^6+1 . Descrambling can be enabled / disabled via the CPU interface for test purposes.

The B2 octets located in the line/multiplex overhead of the SONET/SDH frame is extracted to determine B2 errors. The B2 calculation is a Bit Interleaved Parity $24*N$ (BIP- $24*N$) calculation on each data bit in the frame excluding the section/regenerator overhead. N is determined by the data rate, where N=1 for OC-3/STM-1, N=4 for OC-12/STM-4 and N=16 for OC-48/STM-16. The parity calculation is performed over the line/multiplex overhead and payload octets after descrambling has occurred. The running parity calculation is compared with the extracted B2 octets and an error count is generated. The error count can be selected via the CPU interface, to provide either a bit count or a block count. The B2 error count is passed to the statistics module and is only updated when the LOF alarm is negated.

The M1 octet located in the line/multiplex overhead of the SONET/SDH frame is extracted to determine Remote Error Indication (REI). The M1 octet is latched and passed to the statistics module where it is integrated to maintain a count of the REI errors occurring. An REI alarm is also generated if the M1 octet is non zero. The REI status is accessible via the statistics module.

The K1 and K2 octets located in the line/multiplex overhead of the SONET/SDH frame are extracted and stored in a register for access via the CPU interface. K1 and K2 octets are only updated when the LOF alarm is negated.

The Alarm Indication Signal (AIS) is generated when bits 6 to 8 of the K2 octet contain the value '111'. The Remote Defect Indicator (RDI) is generated when bits 6 to 8 of the K2 octet contain the value '110'. Both the AIS and RDI alarms are validated over 3 or 5 frames dependant on the transport mode selected (SONET or SDH). The transport mode is configured via the CPU interface. The AIS and RDI status is accessible via the statistics module.

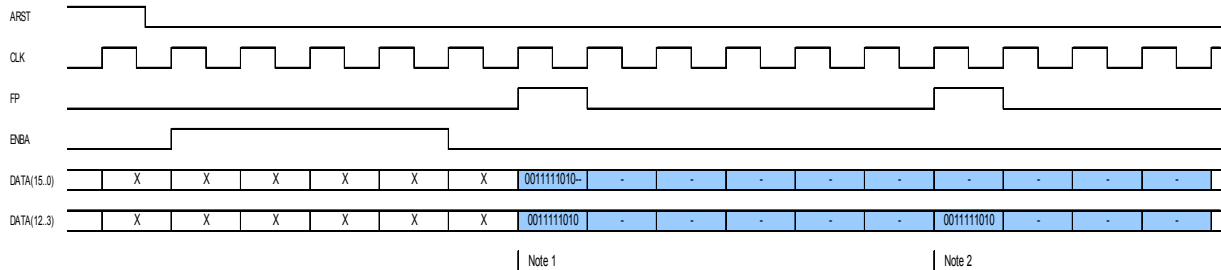
The J0 octet located in the section/regenerator overhead of the SONET/SDH frame can be captured to form a J0 section trace message. The message may be either 16 or 64 bytes in length and is stored in RAM which may be accessed via the CPU interface. The J0 Capture mechanism must be initialised to trigger the capture of a message. Capture commences when a message boundary is found, indicated when the MSB of the J0 octet is '1'. The capture of a message can also be forced such that the message will be captured immediately, regardless of the message boundary. Control of the J0 capture mechanism and indication of capture completion is achieved via the CPU interface.

8B/10B Alignment

In 8B/10B mode the frame pulse is used only for initial bit synchronisation. With a 16 bit bus width, a frame pulse is expected to be aligned with a data word containing the k28.5 character in the 10 most significant bits. This scenario is valid while the external pattern matcher is actively re-aligning the data stream. When the external pattern matcher is not re-aligning the data stream, a frame pulse is still required, but the k28.5 character may or may not be aligned with the 16 bit word. The bit synchronisation process will wait for a frame pulse that is not aligned with the k28.5 character to determine when re-alignment has completed. Selecting a 10 bit bus requires that the frame pulse is aligned with a data word containing the k28.5 character. 8 and 4 bit bus width is not supported in 8B/10B mode.

A byte alignment output (ENBA) is provided to enable an external pattern matcher to bit align the data stream to a k28.5 character. ENBA is asserted for four clock cycles indicating re-alignment is required.

For an input bus width of 16 bits, the internal 16 bit bus must be translated to a 20 bit bus for maximum bandwidth 8B/10B decoding. When a 10 bit bus width is selected, this function must translate the 10 active bits to the 20 bit bus. The bus translation function is configured via the CPU interface.



Note 1 External data re-alignment occurs when ENBA is asserted or for first frame pulse after ENBA has been negated

Note 2 External data re-alignment is disabled and k28.5 character may or may not be aligned in 16 bit mode.

Figure 3 8B/10B Alignment

8B/10B Performance Monitoring

The 20 bit data bus presented to the 8B/10B decoder contains two 8B/10B encoded words. Each 10 bit word is checked to determine if it is a legal 8B/10B code. If the word is not valid, a code error alarm is generated.

For each code word the disparity is determined and compared with a running disparity. If the disparity of the received code word violates the 8B/10B disparity rules, a disparity error alarm is generated.

Code error and disparity error status is accessible via the statistics module. Code errors and disparity errors are also passed to the statistics to provide a running count for each indicator.

Character synchronisation is selectable to provide synchronisation on a single code word containing a comma or synchronisation according to the IEEE 802.3 Annex 36 synchronisation diagram. A loss of synchronisation alarm is generated accordingly and is accessible via the statistics module. Character synchronisation is configured via the CPU interface.

Statistics Collection

The statistics counters are implemented in two banks with one bank actively counting statistics. The alternate bank is accessible to the CPU interface for retrieval of statistic collected during the previous heartbeat interval. A new heartbeat interval is indicated by a pulse on the heartbeat input, initiating a statistic bank switch. At the start of each heartbeat interval, the active bank is first cleared prior to counting any statistics.

For a period of time at the start of each heartbeat interval, the statistics from the previous period must be updated. This period can be up to 96 clock cycles at the system clock frequency. The CPU must wait for this process to complete before retrieving any statistics. Indication of the process completion is provided via the CPU interface.

The statistics module contains 8 counters; each counter is 31 bits, with the 32nd bit defined as a count overflow. If the counter overflows this bit is set and remains set until the next heartbeat period. Since CPU access is limited to 16 bits, two CPU reads will be required to determine the total counter value.

To minimise logic resources required, the statistics counters are mode dependant. The statistics contained in each counter is specific to the mode that has been selected (SONET/SDH or 8B/10B). The following table indicates the statistics contained in each counter.

Counter	SONET / SDH Mode	8B / 10B Mode
1	B1 Errors	N/A
2	REI Errors	N/A
3	B2 Errors (Weight 1)	Code Error 1
4	B2 Errors (Weight 2)	Code Error 2
5	B2 Errors (Weight 4)	Disparity Error 1
6	B2 Errors (Weight 8)	Disparity Error 2
7	B2 Errors (Weight 16)	Loss of Sync
8	B2 Errors (Weight 32)	N/A

For the particular case of the B2 errors, the count is comprised of a series of weighted counts valued at 1, 2, 4, 8, 16 and 32 respectively. The value contained in the B2 error registers must be multiplied with these weights and the sum calculated to obtain the total B2 error count for the current heartbeat interval.

For the particular case of the 8B/10B statistics, code errors and disparity errors, there exists two 32 bit registers for each statistic. These two values must be summed together to obtain the total code error or total disparity error count for the current heartbeat interval.

In addition to counters, the status of the alarm signals are latched within the statistics module over the heartbeat interval. If an alarm occurs at any time during the interval, its occurrence will be detected and the corresponding status bit will be set for the remainder of the heartbeat interval. The alarm status is cleared at the start of each heartbeat period. As with the statistic counters, the alarm status is mode dependent as shown in the following table.

Status Bit	SONET / SDH Mode	8B / 10B Mode
0	LOS	LOS
1	OOF	Loss of Sync
2	LOF	Code Error
3	AIS	Disparity Error
4	RDI	N/A
5	REI	N/A

CPU Interface

The CPU interface provides the control and status access for the core. A generic interface has been designed to allow simple connection to the many processor buses available. The interface is synchronous to the CPU clock (SCLK) and consists of an 8 bit address bus (SA), 16 bit input data bus (SDI), 16 bit output data bus (SDO), data output valid (SDOV), access enable (SEN) and write enable (SWE).

A read cycle is achieved by negating SWE and asserting SEN. The data located in the register indicated by the valid address will appear on SDO and is indicated by SDOV.

A write cycle is achieved by asserting SWE and asserting SEN. The valid data on SDI will be written to the register indicated by the valid address after the rising edge of SCLK occurs.

The minimum pulse width for both SWE and SEN is one clock cycle. SWE and SEN can be asserted for multiple clock cycles; however the data read from or written to the internal registers will updated with the last rising edge of SCLK coinciding with SEN being asserted.

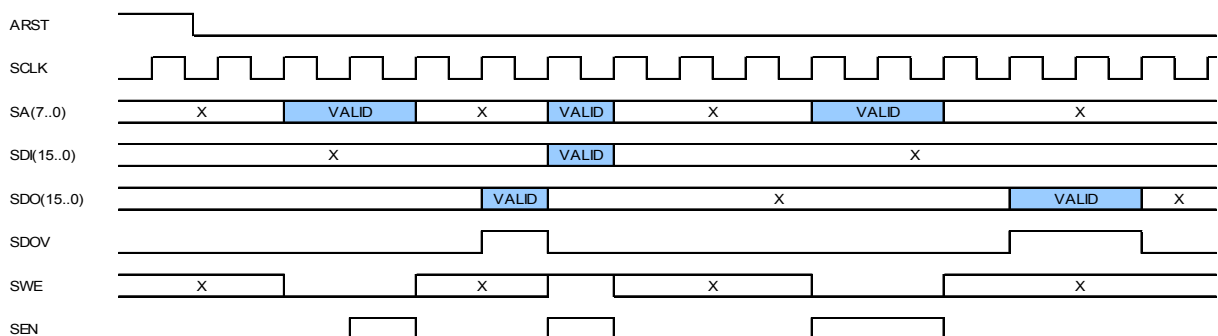


Figure 4 Example CPU Cycles

INTERFACE DESCRIPTION

Symbol	Name	I/O	Level	Description
ARST	Asynchronous Reset	I	H	Asynchronous reset for all modules
CLK	System Clock	I	CP	System clock supporting frequencies up to 155.52MHz
FP	Frame Pulse	I	H	Frame pulse input indicating frame or code word alignment
ENBA	Byte Align Enable	O	H	Byte alignment enable to external data pattern matcher
DATA<15..0>	System Data	I	X	16 bit system data bus
LOS	Loss of signal	I	H	Loss of signal indicator from external hardware
HB	Heartbeat	I	H	Heartbeat pulse for statistics collection
SCLK	CPU Clock	I	CP	CPU interface clock
SA<7..0>	CPU Address Bus	I	X	CPU interface 8 bit address bus
SDI<15..0>	CPU Input Data Bus	I	X	CPU interface 16 bit input data bus
SDO<15..0>	CPU Output Data Bus	O	X	CPU interface 16 bit output data bus
SDOV	CPU Data Output Valid	O	H	CPU interface output data bus valid
SWE	CPU Write Enable	I	H	CPU interface write enable
SEN	CPU Enable	I	H	CPU interface enable

KEY: I = INPUT, O = OUTPUT, C = CLOCK, P = POSITIVE EDGE SENSITIVE, N = NEGATIVE EDGE SENSITIVE, H = ACTIVE HIGH, L = ACTIVE LOW, X = BUS

NOTES

Design Detail

This data sheet provides a general overview of the CORE-PM-2G5. For further technical details including CPU memory map, CPU register definitions and detailed timing diagrams, please contact CALYPTECH via one of the methods detailed below.

Implementation

The CORE-PM-2G5 is available as an EDIF net-list file or VHDL source code, with a constraint file to achieve routing at maximum speed. A VHDL test bench can be supplied to verify operation of the provided implementation of the CORE-PM-2G5.

CALYPTECH CONTACT DETAILS

Support and technical assistance is available for all CALYPTECH Intellectual Property cores.

Address: CALYPTECH Pty Ltd, Suite 4, 486 Lower Heidelberg Road, Heidelberg, Victoria, Australia, 3084	
Telephone: +61 3 9455 1290	Fax: +61 3 9459 9966
Email: info@calyptech.com	Web: http://www.calyptech.com