

## GENERAL DESCRIPTION

The SONET/SDH Framer and Data Aligner core accepts a 64 bit data bus clocked at a nominal 155.52MHz. The core performs SONET/SDH A1/A2 frame detection from an arbitrary alignment and aligns the data to the correct byte and word boundaries. Severely Errored Frame (SEF), Loss of Frame (LOF) and Loss of Signal (LOS) detection is also performed with programmable thresholds. Row and column counters are generated along with the aligned data to enable location of any word in the SONET/SDH frame. Frame alignment status signals are also provided by this core.

The core is fully compliant to Telcordia GR-253-CORE, ANSI T1.105 and ITU-T G.707.

## FUNCTIONAL DESCRIPTION

Incoming SONET STS-192 or SDH STM-64 (concatenated or non-concatenated) data is input to the FRAME FIND block. This block continuously searches all bit locations of each word for valid A1 and A2 bytes. The search is performed every clock cycle and uses the IFRM\_DET\_MODE input to determine whether 3, 12, 48 or 64 A1/A2 pairs are to be checked.

Once a match has been found, the framer state machine immediately enters the PREFRAME state, and resets the internal row and column counters. The alignment in which the A1/A2 pairs were found is also latched, and sent to the WORD ALIGN block that re-aligns the incoming data to both byte and word boundaries.

The framer state machine waits until the next expected frame boundary, and again checks for valid A1/A2 pairs according to the IFRM\_DET\_MODE mask. If a valid framing pattern is found, the state machine enters the INFRAME state and removes the OSEF\_DEFECT alarm. The state machine then checks for a valid framing pattern during each frame using the ISEF\_DET\_MODE mask. This can be set to monitor a different number of A1/A2 pairs than the IFRM\_DET\_MODE mask. If frame errors are detected, the SEF counter starts incrementing. This counter is reset whenever a correct framing pattern is detected. If the SEF counter reaches the programmable ISEF\_SET\_THR threshold, the framer state machine returns to the HUNT state, and asserts the OSEF\_DEFECT alarm.

Whenever the OSEF\_DEFECT alarm is asserted, a counter inside the LOF DETECT block increments every 125µs. Once the counter reaches the programmable ILOF\_SET\_THR threshold, OLOF\_DEFECT is asserted. This alarm remains active until the SEF defect is cleared, and the framer remains INFRAME continuously for the programmable ILOF\_CLR\_THR threshold.

A separate LOS DETECT block inside the core continuously monitors the incoming data for strings containing all zeroes. The programmable ILOS\_SET\_THR threshold determines how long the all zeroes string must persist before the OLOS\_DEFECT alarm is asserted. This alarm is cleared in one of two ways depending on the ILOS\_CLR\_CRIT input. The first method clears the alarm after receiving two valid frame alignment patterns with no occurrence of an all zeroes string qualifying for the ILOS\_SET\_THR threshold. The second method clears the alarm after no occurrence of an all-zeroes string qualifying for the ILOS\_CLR\_THR threshold.

## INTERFACE CONFIGURATION

### FRAMER / DATA ALIGNER

▶ RESET	
▶ CLK	
▶ IDATAIN<63..0>	ODATAOUT<63..0>
▶ IFRM_DET_MODE<1..0>	OSEF_DEFECT
▶ ISEF_DET_MODE<1..0>	OLOF_DEFECT
▶ ISEF_SET_THR<2..0>	OLOS_DEFECT
▶ ISHORT_FRM_MODE	OHUNT
▶ ILOF_SET_THR<4..0>	OPREFRAME
▶ ILOF_CLR_THR<4..0>	OROW_COUNT<3..0>
▶ ILOS_SET_THR<7..0>	OCOL_COUNT<11..0>
▶ ILOS_CLR_THR<7..0>	
▶ ILOS_CLR_CRIT	

## FEATURES

- Single cycle A1/A2 search algorithm provides the fastest possible frame alignment time
- Programmable 3, 12, 48 or 64 pair A1/A2 search mask
- Detects SEF, LOF and LOS alarm conditions
- Programmable set and clear thresholds for LOF, LOS and programmable set threshold for SEF
- Aligns incoming data to correct byte and word boundaries
- Row and Column counter outputs aligned with data output
- Short frame mode for simulation
- Suitable for FPGA and ASIC target technology
- GR-253-CORE, T1.105 and G.707 compliant

## TARGET APPLICATIONS

- SONET / SDH 10Gb/s network equipment
- SONET / SDH 10Gb/s test equipment

**BLOCK DIAGRAM**

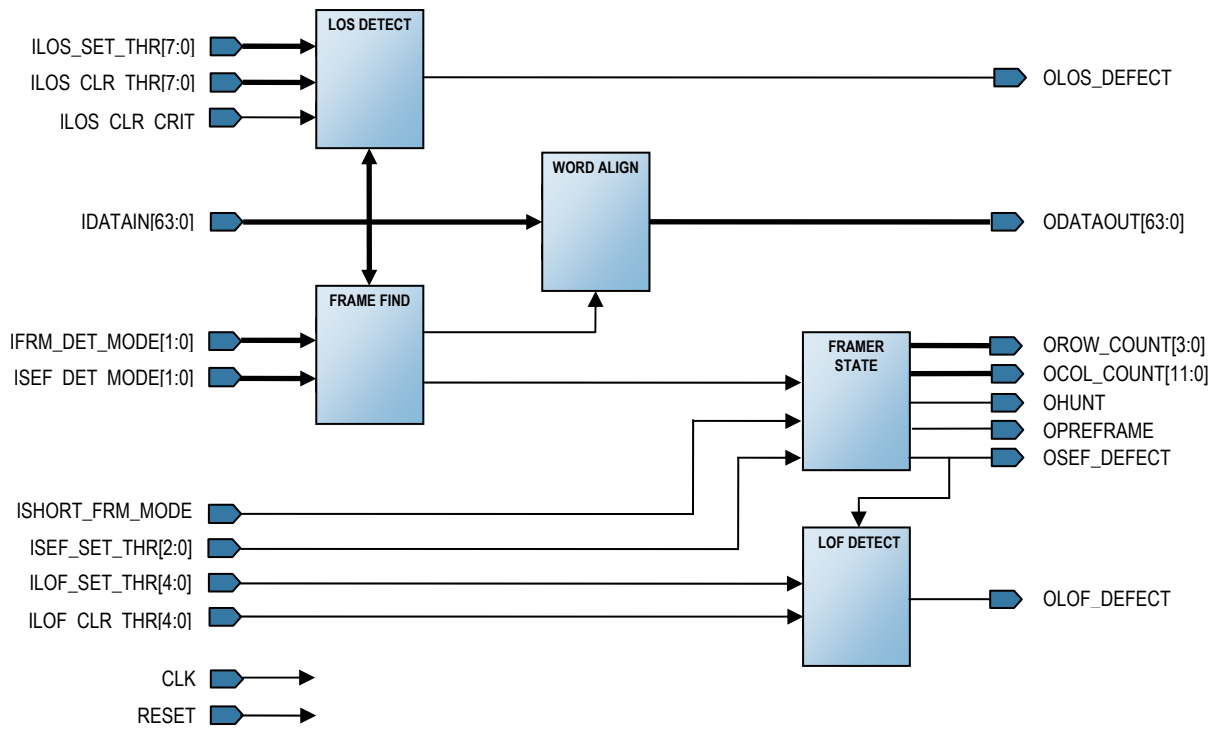


Figure 1 Block Diagram

## INTERFACE DESCRIPTION

Symbol	Name	I/O	Level	Description
CLK	Clock	I	CP	Continuous clock input to all internal flip flops
RESET	Asynchronous Reset	I	H	Asynchronous reset to all internal flip flops
IDATAIN[63:0]	Input SONET / SDH framed data	I	X	Demultiplexed input data bus from a SFI-4 de-serialiser or similar. SONET / SDH frame alignment is assumed to be arbitrary
IFRM_DET_MODE[1:0]	Frame detect mode	I	X	Sets the number of A1/A2 pairs to check when searching for and validating frame alignment: '00' 3 pairs checked '01' 12 pairs checked '10' 48 pairs checked '11' 64 pairs checked
ISEF_DET_MODE[1:0]	SEF detect mode	I	X	Sets the number of A1/A2 pairs to check when analysing frames for SEF detection: '00' 3 pairs checked '01' 12 pairs checked '10' 48 pairs checked '11' 64 pairs checked
ISEF_SET_THR[2:0]	SEF set threshold	I	X	Sets the number of consecutive severely errored frames before SEF is declared
ISHORT_FRM_MODE	Short frame mode	I	H	When asserted, the frame size is reduced to only the overhead portion of the frame for simulation purposes. The column counter is reset following the last overhead word of each row (the row counter operates normally)
ILOF_SET_THR[4:0]	LOF set threshold	I	X	Sets the threshold, in units of 125µs that Loss of Frame is declared after OSEF_DEFECT is asserted
ILOF_CLR_THR[4:0]	LOF clear threshold	I	X	Sets the threshold, in units of 125µs that Loss of Frame is cleared after OSEF_DEFECT is de-asserted
ILOS_SET_THR[7:0]	LOS set threshold	I	X	Sets the threshold, in units of 0.41µs (64 clock cycles) that Loss of Signal is declared after a continuous string of zeroes on the input data bus
ILOS_CLR_THR[7:0]	LOS clear threshold	I	X	Sets the threshold, in units of 0.41µs (64 clock cycles) that Loss of Signal is cleared after a continuous string of non-zeroes on the input data bus
ILOS_CLR_CRIT	LOS clear criteria	I	H	Selects the criteria for clearing the Loss of Signal alarm: '0' LOS is cleared when two valid framing patterns are detected with no occurrence of an all zeroes pattern qualifying for the ILOS_SET_THR threshold '1' LOS is cleared when there is no occurrence of an all zeroes pattern qualifying for the ILOS_CLR_THR threshold
ODATAOUT[63:0]	Aligned SONET / SDH output data	O	X	Output data that has been byte and word aligned
OSEF_DEFECT	SEF alarm	O	H	Severely Errored Frame defect alarm
OLOF_DEFECT	LOF alarm	O	H	Loss of Frame defect alarm
OLOS_DEFECT	LOS alarm	O	H	Loss of Signal defect alarm
OHUNT	Framer HUNT state indicator	O	H	Asserted when the framer state-machine is in the HUNT state. This state indicates that the framer is searching for frame alignment.
OPREFRAME	Framer PREFRAME state indicator	O	H	Asserted when the framer state-machine is in the PREFRAME state. This state indicates that the framer has found a correct framing pattern and is waiting to validate the next expected pattern.
OROW_COUNT[3:0]	SONET / SDH frame row counter	O	X	Indicates the current row (0 - 8) of the SONET / SDH frame.
OCOL_COUNT[11:0]	SONET / SDH frame column counter	O	X	Indicates the current column (0 - 2,159 or 0 - 71 in short frame mode) of the SONET / SDH frame.

KEY: I = INPUT, O = OUTPUT, C = CLOCK, P = POSITIVE EDGE SENSITIVE, N = NEGATIVE EDGE SENSITIVE, H = ACTIVE HIGH, L = ACTIVE LOW, X = BUS

#### NOTES

The framer and data aligner core is also available in STS-768/STM-256 (256-bit data bus) and STS-48/STM-16 (16-bit data bus) versions. The part numbers of these cores are as follows:

- CORE-FRM-768. SONET/SDH STS-768/STM-256 Framer and Data Aligner
- CORE-FRM-48. SONET/SDH STS-48/STM-16 Framer and Data Aligner

Please contact Calyptech if other configurations of this core are required.

#### CALYPTECH CONTACT DETAILS

Support and technical assistance is available for all CALYPTECH Intellectual Property cores.

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