

## GENERAL DESCRIPTION

The TDM Switch core provides a 16,384 by 16,384 channel, non-blocking switch targeting telecommunications applications. Data is organized into 32 streams on the input and 32 streams on the output. Each stream operates at 32.768Mb/s and uses a data format compatible with the ST-BUS protocol. Each stream transports 512 channels, with each channel supporting a bandwidth of 64Kb/s. Lower stream rates are possible for compatibility with other ST-BUS devices.

Data passing through the switch has a latency of two frames. The timing of the output frames are locked to the input frame.

## FUNCTIONAL DESCRIPTION

The switching function operates on individual channel timeslots, which are written to a Data Memory sequentially. A Connection Memory is configured to control the order in which the timeslots appear on the output of the Data Memory.

### Connection Memory

The switch uses a Connection Memory to store the map between the input stream timeslots and the output stream timeslots. The Connection Memory is organized as a 16,384 x 14 bit array. The address format of a location in the Connection Memory represents a source stream and channel number, while the data value in that addressed location represents the destination stream and channel number.

Broadcast switching is supported by mapping a single source channel onto multiple destination channels in the Connection Memory.

This memory may be written to at any time to update the switch configuration of a given channel/stream without affecting the operation of other channels/streams.

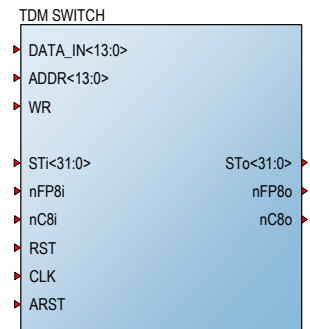
### Data Memory

Data is written sequentially, with each read access controlled by the Connection Memory.

### Memory Interface

The channel mapping is written into the Connection Memory via the Memory Interface, which provides a simple synchronous interface.

## INTERFACE CONFIGURATION



## FEATURES

- 32 input and 32 output streams compliant with ST-BUS protocol
- Non blocking switch matrix of 16,384 x 16,384 channels
- 32.768Mb/s stream data rate
- Unidirectional switching
- Bidirectional switching supported using two instances of the core
- Switch can be reconfigured while transferring data
- 131.072MHz core clock
- Xilinx Virtex-II / Virtex-II Pro FPGA target technology
- Resource utilization is 600 slices and 30 block RAMs

## BLOCK DIAGRAM

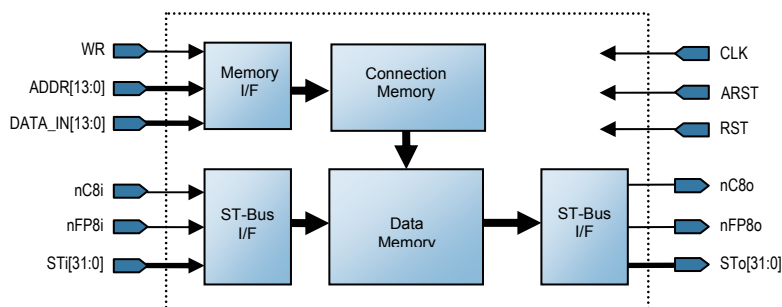


Figure 1 Block Diagram

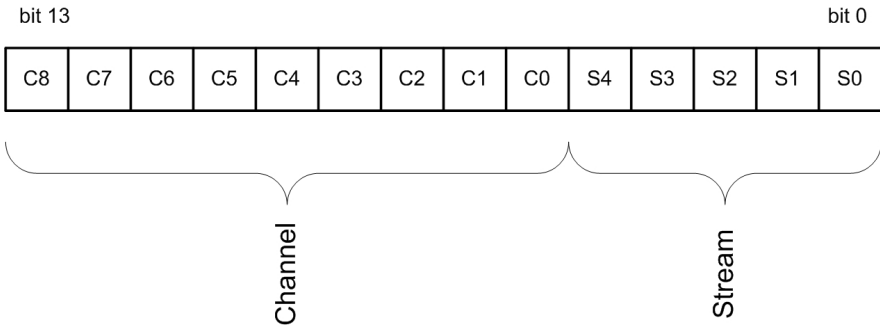
## TARGET APPLICATIONS.

- Backplane Switches.

## REGISTER MAP

The TDM switch core is accessed using a synchronous memory interface, which makes efficient use of FPGA resources. This provides a 14-bit wide data bus and a 14-bit wide address bus, for a total address space of 16K words.

Address	Name	Access	Width	Description
0000-3FFF	CONN	WO	14	The connection memory defines the mapping of input streams and channels to output streams and channels. Bits 0-4 of the address bus specify the input stream number (0-31) and bits 5-13 of the address bus specify the input channel number (0-511). The data value written specifies the output stream and channel number. Bits 0-4 of the data word specify the output stream number (0-31) and bits 5-13 of the data word specify the output channel number (0-511).



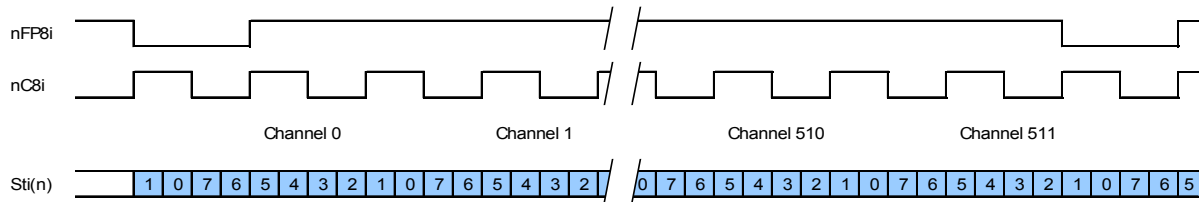
## INTERFACE DESCRIPTION

Symbol	Name	I/O	Level	Description
ARST	Asynchronous Reset	I	H	Asynchronous reset, all internal state elements are reset to '0'. This input must be tied to '0' if not used
RST	Synchronous Reset	I	H	Synchronous reset, all internal state elements reset to '0'
CLK	Clock	I	CP	131.072MHz continuous clock
DATA_IN[13:0]	Data	I	X	Synchronous data for configuration of the switch core
ADDR[13:0]	Address	I	X	Synchronous address for register selection within the switch core
WR	Write Enable	I	H	Enable writing of data into the switch core
STI[31:0]	Input Stream Data	I	X	32 input data streams at 32.768Mb/s formatted to the ST-BUS protocol
nFP8i	Input Frame Pulse	I	L	8KHz frame pulse used to align the incoming data to channel boundaries
nC8i	Input Clock Reference	I	L	8.192MHz clock must be synchronous to CLK for correct operation
STO[31:0]	Output Stream Data	O	X	32 output data streams at 32.768Mb/s formatted to the ST-BUS protocol
nFP8o	Output Frame Pulse	O	L	8KHz frame pulse indicating frame alignment of the output data
nC8o	Output Clock Reference	O	L	8.192MHz clock synchronous to CLK

KEY: I = INPUT, O = OUTPUT, C = CLOCK, P = POSITIVE EDGE SENSITIVE, N = NEGATIVE EDGE SENSITIVE, H = ACTIVE HIGH, L = ACTIVE LOW, X = BUS

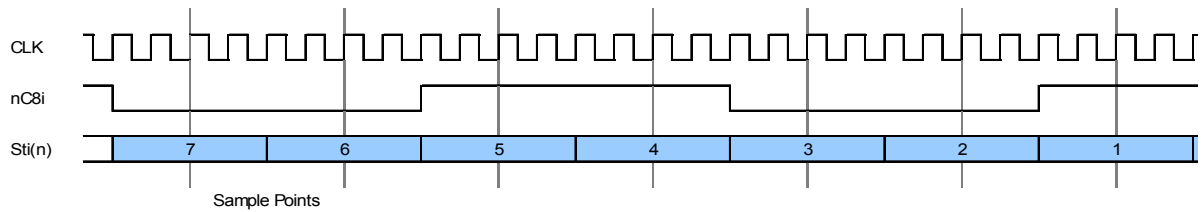
**TIMING DIAGRAMS**

**Figure 2 ST-BUS Data Format**



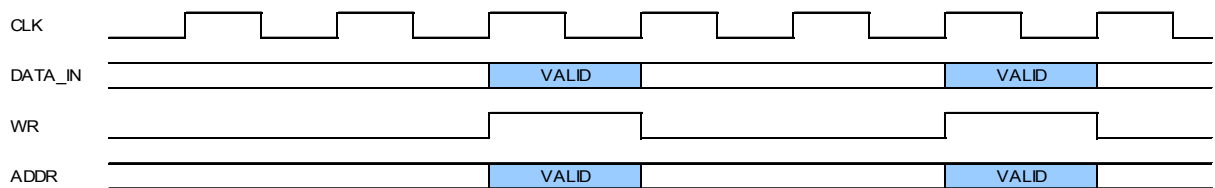
- Note 1** Data is transmitted and received MSB first in the ST-BUS protocol.
- Note 2** The frequency of nC8i is 8.192MHz.
- Note 3** The frame pulse (nFP8i) arrives at 8KHz, with a duration of 122ns.
- Note 4** The data rate over each stream STi(n) is 32Mb/s.
- Note 5** The frame pulse and clock outputs use identical timing formats as the inputs

**Figure 3 ST-BUS Data Sampling**



- Note 1** The STi(n) inputs are sampled at the centre of each bit position by the core.
- Note 2** The frequency of nC8i is 8.192MHz and the frequency of CLK is 131.072MHz.

**Figure 4 Write Access Timing**



- Note 1** Data accesses are all synchronized to the CLK input (131.072MHz)

**DESIGN NOTES****ST-BUS**

The ST-BUS is a proprietary protocol of Zarlink Semiconductor.

**Frame Alignment**

The frame pulse provides a reference for frame alignment. Within each frame, a single channel occupies one octet. The input may be bit-shifted to accommodate skew on a per-stream basis.

**Timing**

The core requires a 131.072MHz global clock. This must be provided externally and may be derived using an optional DCM in the core.

**Implementation**

The TDM Switch core is available as an EDIF net-list file or VHDL source code, with a constraint file to achieve routing at maximum speed. A VHDL test bench can be supplied to verify operation of the provided implementation of the TDM Switch core.

**Additional Features**

The TDM Switch core may be extended to allow each stream input to be delayed or advanced individually by a fixed amount if required.

**CALYPTECH CONTACT DETAILS**

Support and technical assistance is available for all CALYPTECH Intellectual Property cores.

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