

GENERAL DESCRIPTION

The CRC32 core consists of a 256-bit wide CRC32 calculator intended for use in OC-768 applications. It uses the standard CRC32 polynomial shown below;

$$x^{32}+x^{26}+x^{23}+x^{22}+x^{16}+x^{12}+x^{11}+x^{10}+x^8+x^7+x^5+x^4+x^2+x+1$$

The CRC32 core targets a Xilinx Virtex 2 Pro FPGA and has been optimised for clock rates up to 180MHz. This clock speed provides the ability to process data at 40Gb/s data rates. Incoming packets may have their first and last octets aligned to any octet boundary on the 256-bit word. All packet sizes are supported, with a restriction on the maximum packet rate being a limit of one packet per clock cycle.

All inputs and outputs are synchronous to the CLK input, except the ARST input.

FUNCTIONAL DESCRIPTION

Transmit

In a typical application of a transmit block in a communications system, the CRC32 bus output contains the CRC32 value to append to the packet data leaving the core. Control signals are reproduced at the outputs, with a delay matching the latency of the CRC32 calculation. The CRC32 value may be externally shifted and inserted into a 4 octet space trailing the packet.

Receive

In a typical application of a receive block in a communications system, the CRC32 bus output contains the CRC32 value of the processed packet data. This value must be externally compared with the expected CRC32 within the packet. If the comparison is true, then the CRC32 check was correct, otherwise there was an error in the packet data. The expected CRC32 is not extracted from the packet.

Timing

The CRC32 Core is a pipelined design to achieve high clock speeds. The core latency is a constant value of 40 clock cycles for the Xilinx Virtex 2 Pro target technology.

BLOCK DIAGRAM

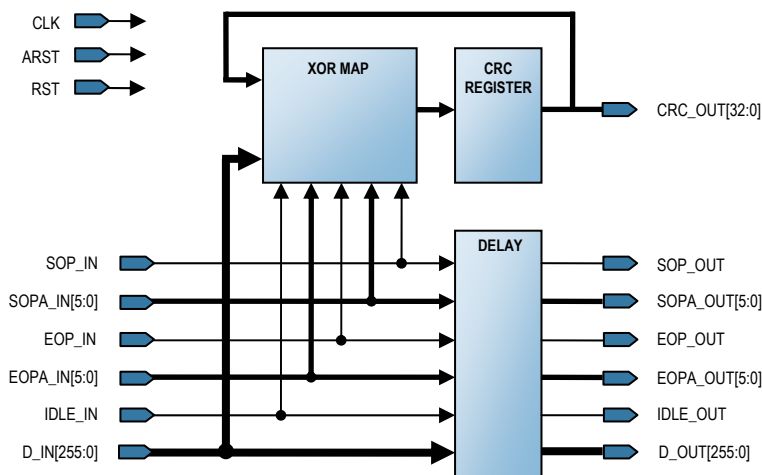
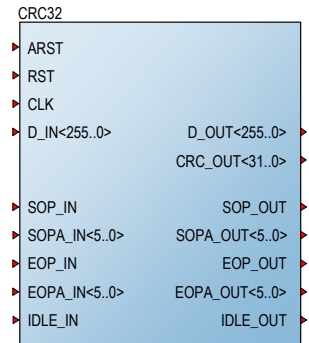


Figure 1 Block Diagram

INTERFACE CONFIGURATION



FEATURES

- **CRC32 Polynomial**
 $x^{32}+x^{26}+x^{23}+x^{22}+x^{16}+x^{12}+x^{11}+x^{10}+x^8+x^7+x^5+x^4+x^2+x+1$
- **180MHz core clock speed**
- **256-bit wide data bus**
- **SOP and EOP aligned to any octet boundary within bus**
- **Supports all packet sizes**
- **Packet rate up to one per clock cycle, or 180 million packets per second**
- **Xilinx Virtex 2 Pro FPGA target technology**
- **Resource utilization is 5500 slices**
- **Incoming signals replicated at output with identical latency to CRC32 function**

TARGET APPLICATIONS

- **OC-768 Telecommunications Systems**
- **40Gb/s Data Processing systems**

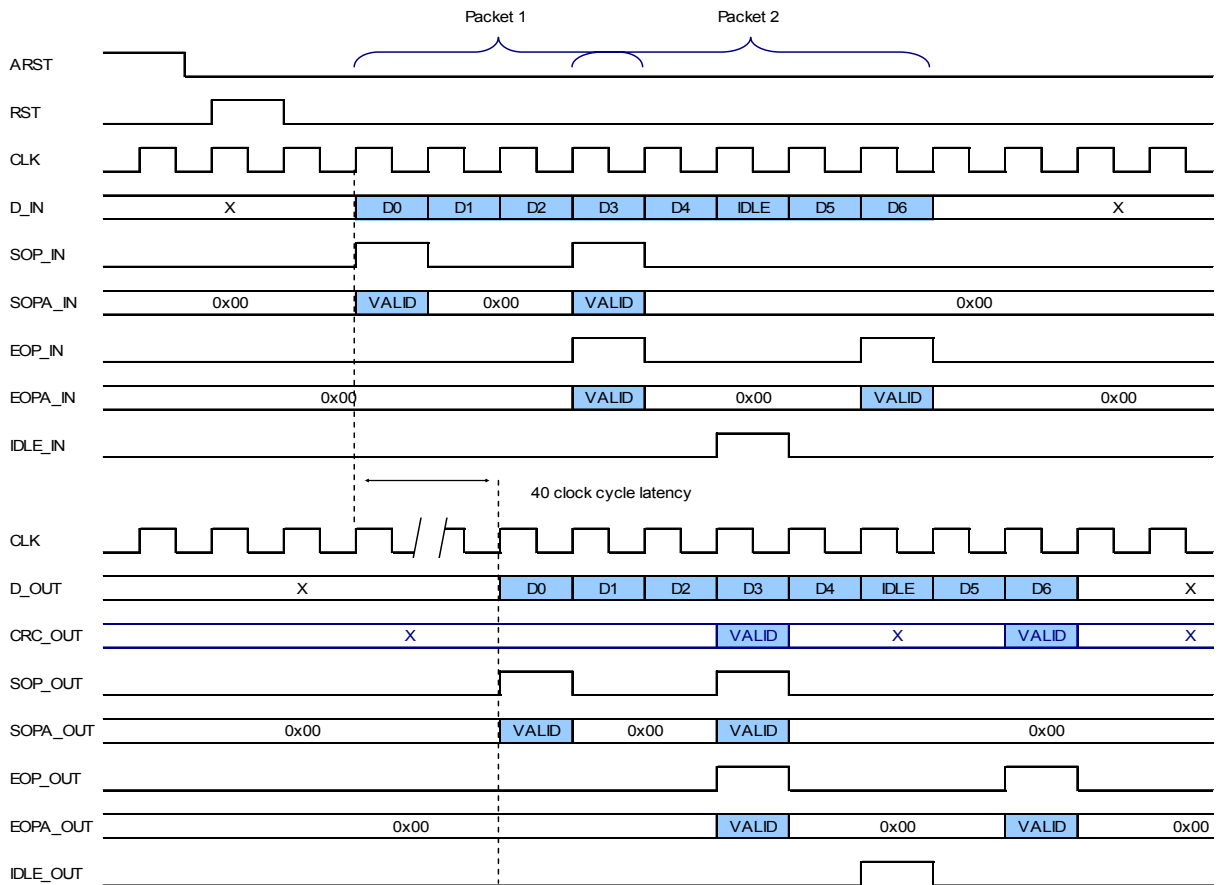
INTERFACE DESCRIPTION

Symbol	Name	I/O	Level	Description
ARST	Asynchronous Reset	I	H	Asynchronous reset, all internal state elements are cleared. This input must be tied to '0' if not used
RST	Synchronous Reset	I	H	Synchronous reset, all internal state elements are cleared
CLK	Clock	I	CP	Continuous clock input
D_IN[255:0]	Data Input	I	X	256-bit data input bus
SOP_IN	Start of Packet Input	I	H	Start of packet bus cycle indicator
SOPA_IN[5:0]	Start of Packet Alignment Input	I	X	Start of packet bus cycle alignment indicating the position within the bus of the first octet in the new packet
EOP_IN	End of Packet Input	I	H	End of packet bus cycle indicator
EOPA_IN[5:0]	End of Packet Alignment Input	I	X	End of packet bus cycle alignment indicating the position within the bus of the last octet in the current packet. Note that SOP and EOP bus cycles may coincide, provided there is no overlap in the used octet regions in the data bus for each packet. This bus is 6 bits wide to allow for a packet ending on the 31 st octet, which will require EOPA_IN to be 0x20
IDLE_IN	Idle Cycle Input	I	H	Idle bus cycle indication. Data input is ignored and any partial CRC is left unchanged
D_OUT[255:0]	Data Output	O	X	256-bit data output bus. Data is delayed by the core latency
CRC_OUT[31:0]	CRC32 Output	O	X	32-bit CRC result output bus. Contains the CRC32 value calculated over the range defined by the start of packet indication and the end of packet indication
SOP_OUT	Start of Packet Output	O	H	Start of packet indicator aligned with CRC_OUT
SOPA_OUT[5:0]	Start of Packet Alignment Output	O	X	Start of packet alignment indicator aligned with CRC_OUT
EOP_OUT	End of Packet Output	O	H	End of packet indicator aligned with CRC_OUT
EOPA_OUT[5:0]	End of Packet Alignment Output	O	X	End of packet alignment indicator aligned with CRC_OUT

KEY: I = INPUT, O = OUTPUT, C = CLOCK, P = POSITIVE EDGE SENSITIVE, N = NEGATIVE EDGE SENSITIVE, H = ACTIVE HIGH, L = ACTIVE LOW, X = BUS

TIMING DIAGRAM

Figure 2 CRC Timing



- Note 1** EOP of Packet 1 occurs in the same cycle as SOP of packet 2. This requires that EOPA_IN < SOPA_IN in this cycle.
- Note 2** On non SOP bus cycles, SOPA_IN must be 0x00 for the CRC32 core to operate correctly.
- Note 3** On non-EOP bus cycles, EOPA_IN must be 0x00 for the CRC32 core to operate correctly.

NOTES**Packet Alignment**

The EOP of one packet and the SOP of the next packet may coincide on a single bus cycle provided that the SOPA and EOPA do not create any contention on the data bus inputs due to overlap. The EOP alignment points to the octet after the last one in the current packet. Therefore a packet ending on the last octet of the bus cycle will have an EOPA value of 0x20. This allows correct processing of zero-byte length packets.

Implementation

The CRC32 core is available as an EDIF net-list file or VHDL source code, with a constraint file to achieve routing at maximum speed.

Additional Features

The CRC32 core can be made to accept nonzero SOPA_IN and EOPA_IN values on non SOP or EOP cycles at the expense of increased Slice usage. The core can be customized for Transmit CRC32 Appending or Receive CRC32 Checking, if required by the user.

CALYPTECH CONTACT DETAILS

Support and technical assistance is available for all CALYPTECH Intellectual Property cores.

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